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SUBJECT AREAS

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Field Programmable Droplets Array: An Active-matrix digital microfluidics platform for field programmable high-throughput digitalized liquid handling

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Digital liquid sample handling is an enabling tool for cutting-edge life-sciences research. Similar to Field Programmable Gate Arrays (FPGA) in Integrated Circuits, we present here an active-matrix thin-film electronics-based digital microfluidics system, which will be henceforth referred to as Field Programmable Droplets Arrays (FPDA). The system contains 256 × 256 pixels in an active area of 10.65 cm^2, which is capable of manipulating thousands of individually addressable liquid droplets simultaneously. By leveraging a customised TFT-based circuit design solution, it becomes possible to programmatically manipulate droplets at the pixel level. The minimum achievable droplet volume is around 0.5 nl, which is two orders of magnitude smaller than the state-of-the-art reported[1]. The movement of droplets can be either pre-programmed or controlled in real-time. The FPDA system shows great potential of the ubiquitous thin-film electronics technology in digital liquid handling. These efforts will make it possible to

create a true programmable lab-on-a-chip device to enable great advances in life science research.

For decades, Very Large-Scale Integrated Circuits (VLSI) has greatly changed people's lives and paved the way to the digital era[2,3]. There are two broad categories of VLSI: Application Specific Integrated Circuits (ASIC) and Field Programmable Gate Arrays (FPGA)[4]. ASICs are customized designs targeted to solve specific tasks, while FPGA can be reprogrammed to meet the desired application specifications or functionality requirements[5]. Due to its programmability and flexibility, FPGAs tend to be preferred for many different applications and markets.

Recently, numerous Lab-on-a-Chip (LOC) platforms have emerged along with innovative technologies for various application areas[6-8]. LOCs can also be divided into two broad categories. First is the traditional microfluidics chip based on custom micro-channel designs, that will be referred to as integrated fluidic circuits (IFC)[9]. IFC have been in continuous development for more than 20 years towards not only the LOC, but also the micro-Total Analysis System (μTAS)[10]. While there are several unavoidable problems restricting its practical application, for instance most IFC require a micro-pump for driving the liquid, hence this greatly increases the size and complexity of the platform; the liquid in IFC is usually continuous, or, even if discrete droplets can be generated, the droplets are not individually addressable; the micro-channels or micro-structures in IFC have a low yield, hence increasing its fabrication cost and hindering the commercial mass production[11-13].

It`s therefore necessary to build a new type of LOC which is not subject to the limitations mentioned above. Firstly, overcoming the one-dimensional restriction of micro-channel is necessary to allow the free movement of droplets in a two-dimensional planar surface. To solve this, droplet manipulation is electrically driven using a method called electrowetting-on-dielectric (EWOD)[14]. EWOD is a physical phenomenon which allows for the manipulation of liquid droplets by applying an electric field to change the wettability of the surface[15]. Therefore, by utilizing an

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electrodes array, water droplets can be manipulated freely on the electrode array surface[16]. Due to its programmatic nature, much like the FPGA, will be referred to as Field Programmable micro-Droplet Array (FPDA).

IFC usually involve the use of lithography to create micro-channels and reservoirs on a substrate, which is then bonded to another substrate either thermally or chemically to create a watertight seal. In comparison, the FPDA has no prefabricated micro-channels or micro-structures and each droplet on the FPDA could be addressed and controlled independently, thus achieving more flexible and complex droplets operations[17]. Additionally, the fabrication of FPDAs is based on standard thin-film processes, which is more mature and precise resulting in larger mass market production scalability[18,19]. This makes FPDAs a more attractive solution in a wider range of applications whereas beyond the ability of conventional IFC.

Active-matrix FPDA

Most of the existing FPDA systems are based on passive electrode arrays, in which each electrode connects to the peripheral electronics directly. Due to the space limitation of driving signals and layout wiring, the scalability issues greatly restrict the scale of the passive-matrix electrode array. Active matrix (AM) technology provides a perfect solution for addressing this issue[20]. In an AM array, pixel circuits contain electronic switches and capacitors to store a logic voltage. Each pixel can be addressed by row and column signal scanning, thus realizing independent pixel control and scalability of the AM array. The additional benefit of the AM technology is for an array sized N (row) × M (column) is addressable by only N + M control signals. All the addressable pixels can be programmed to provide sequenced patterns for liquid droplets on chip to realise a FPDA for lab-on-a-chip applications (Supplementary Section 1).

Depending on the basic micro switch we use, there are two methods to realize FPDA, the first is TFT, while the other method is based on complementary metal oxide semiconductor (CMOS). The TFT-based FPDAs are generally fabricated on glass

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substrate, while the CMOS-based chips are fabricated on silicon wafer, thus their fabrication cost is not in the same order of magnitude. In addition, the TFT-based FPDA chip possesses the ability of large area fabrication process and high optical transparency, which cannot be achieved on a traditional silicon wafer[21-23]. These benefits indicate that, a TFT-based device is more suitable to use for FPDA.

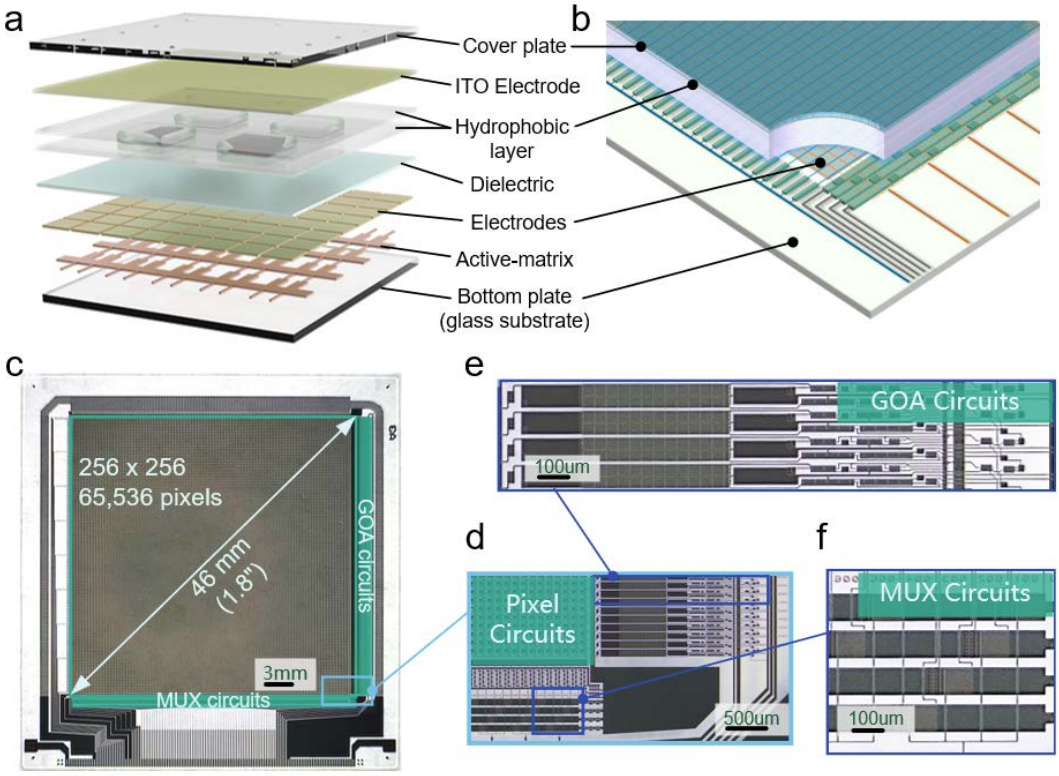

Figure 1. Design of an active-matrix digital microfluidics based FPDA system. a, Cross-section view; b, 3D view; c, photograph of a 256×256 pixels FPDA; d, picture of a part of the array; e, picture of the GOA circuits; f, picture of the MUX circuits.

A full view of the FPDA chip is shown in Fig 1f, and the details of decomposed parts can be seen in Fig 1c, 1d & 1e. The layout of FPDA chip can be seen in the Supplementary Section 2. As mentioned before, AM technology is an ideal method for solving the scalability issues present in PM matrix. Different functional circuits are designed to realize a massive scale active-matrix electrodes array by further reducing row and column driving signals. In AM matrix, each pixel can be individually addressed by the row and column scanning method, in which the row scan signals are

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transmitted line by line so it is possible to use a shift register for generating and transmitting the row scan signals. The shift register circuits are also referred as to gate on array (GOA) and located on one side of the electrodes array (shown in Fig 1d). The GOA circuits can generate several hundreds of driving signals serially, while the GOA itself needs only 4 driving signals, thus it significantly reduces the number of external row driving signals. The outputs of column data is in parallel, and another circuit is designed to reduce the column driving signals instead of the serial GOA circuits. The circuit is simple and effective, and several TFTs control a column data signal into the pixel array. By turning each TFT device on in sequence, one data signal can be divided into several parallel driving signals. Here 4 TFTs is used to control one data signal, so the number of column-driving signals has been reduced by nearly 4 times. With these modifications, it is possible to address 65,536 pixels using less than 80 driving signals (Supplementary Section 3).

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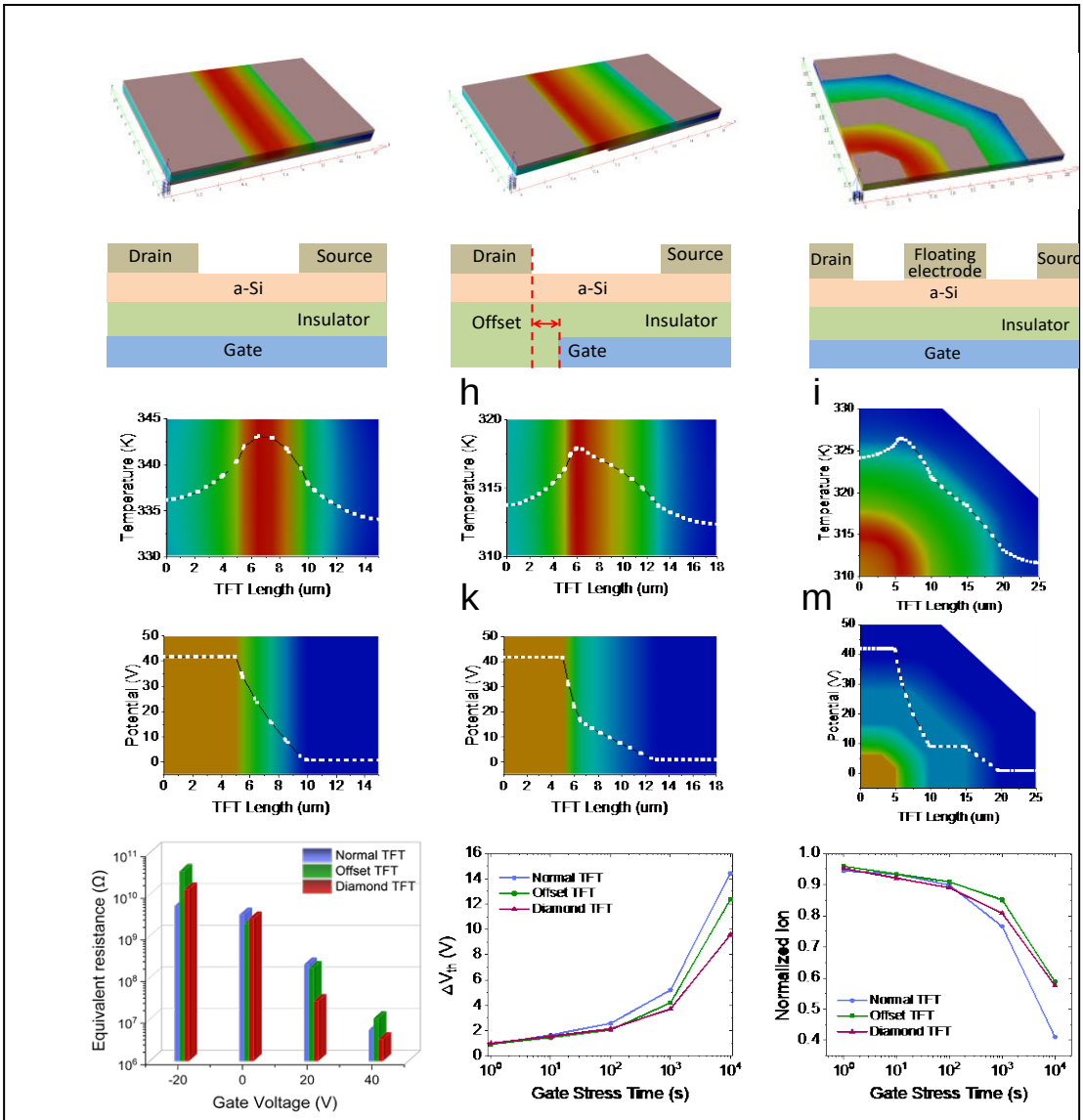

Figure 2. Optimization of the TFT device in FPDA. a~c, Stereogram of temperature distribution in normal TFT, offset TFT and diamond TFT; d~f, cross section view of the three TFTs; g~i, temperature curve with TFT length of the three TFTs; j~m, potential variation with TFT position in the three TFTs; n, equivalent resistance of different TFTs under different gate voltages; p, threshold voltage stability of different TFTs under gate positive bias stress; q, on current stability of the three TFTs under different gate positive bias stress time.

Thin-film transistor device structure optimization

In order to realize large-area droplets manipulation, a well-designed driving strategy is necessary, which requires the design of TFT device and pixel circuit. The driving voltage requirement in FPDA is different from other applications, such as high voltage transmission and pixel voltage stability. We compared and simulated the TFT device and pixel circuit of the FPDA chip, and Fig 2a~2i shows the TCAD simulation results of

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channel temperature distribution and voltage drop across different TFT devices. Fig 2a is the 3D structure of the normal bottom gate bottom contact (BGBC) TFT device, which is the common structure of amorphous silicon. The channel width/length (W/L) of the BGBC TFT is 20 μm / 6 μm. When a high voltage up to 50 V is applied to the gate electrode and 40 V to the drain electrode, a drain current of around 100 μA is produced. High drain current stress causes the self-heating effect of the TFT device, which leads to performance degradation such as threshold voltage (Vth) shift, channel current drop, transconductance distortion, etc. Therefore, to improve the high-voltage performance of TFT device, the conventional method is to place a high-resistance area between the drain and channel, namely drain-offset[24]. Fig 2b shows a typical structure of drain-offset TFT, where the gate electrode does not overlap with the drain electrode. The channel width of the offset TFT is 20 μm, with an offset length of 3 μm and a channel length of 6 μm. The drain-offset area could divide the high drain voltage applied to the channel, thus reducing the high drain current transferred in the channel. The disadvantage of a drain-offset TFT device is that the resistance of the offset area is very large, which increases the overall gate-on resistance and reduces the total channel on-current.

To address the above, a new structure of TFT was designed, as shown in Fig 2c & 2f, which will be referred to henceforth as the diamond TFT structure. The diamond TFT comprises of two channels separated by a floating electrode. Both channels have a different width but are of equal length of 6 μm. The width of the inner most channel is 14 μm, whereas the width of outermost channel is 30 μm. Two channels in series can withstand the high voltages applied on the drain electrode, thus reducing the transverse electric field strength. Compared to the traditional single channel TFT, the floating electrode in diamond TFT could form a balanced electric field inside the channel, which improves the stability of the TFT device.

Fig.2g~2i show the temperature-distribution simulation of the three TFT devices. Due to the different dimensions of the three devices, the device sizes were normalized. When the same voltage is applied to all three types of TFT devices, the channel

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temperature of conventional single channel device is the highest, and the channel temperature of diamond devices is between the offset device and single channel device. Fig.2j~2m show the potential distribution simulation of the three TFT devices. The channel of offset TFT serially connected to a high resistance region results in a significant voltage drop in that region. The diamond TFT also has a voltage drop in the inner channel, while the current transmission capability is better than the offset TFT device. To further compare the characteristics differences of the three TFT devices, the output curve of the TFT device was measured and the equivalent resistance was calculated. As shown in Fig.2n, when the gate is open, the channel resistance of diamond TFT is smaller than the offset TFT and the normal TFT, which means that the diamond TFT has a better current transmission characteristic. Additionally, the diamond TFT has better positive bias stress (PBS) stability, as shown in Fig.2p & 2q, after 10k seconds, the threshold voltage (Vth) shift of diamond TFT is less than 10V, while other TFTs are more than 10V (Supplementary Section 4).

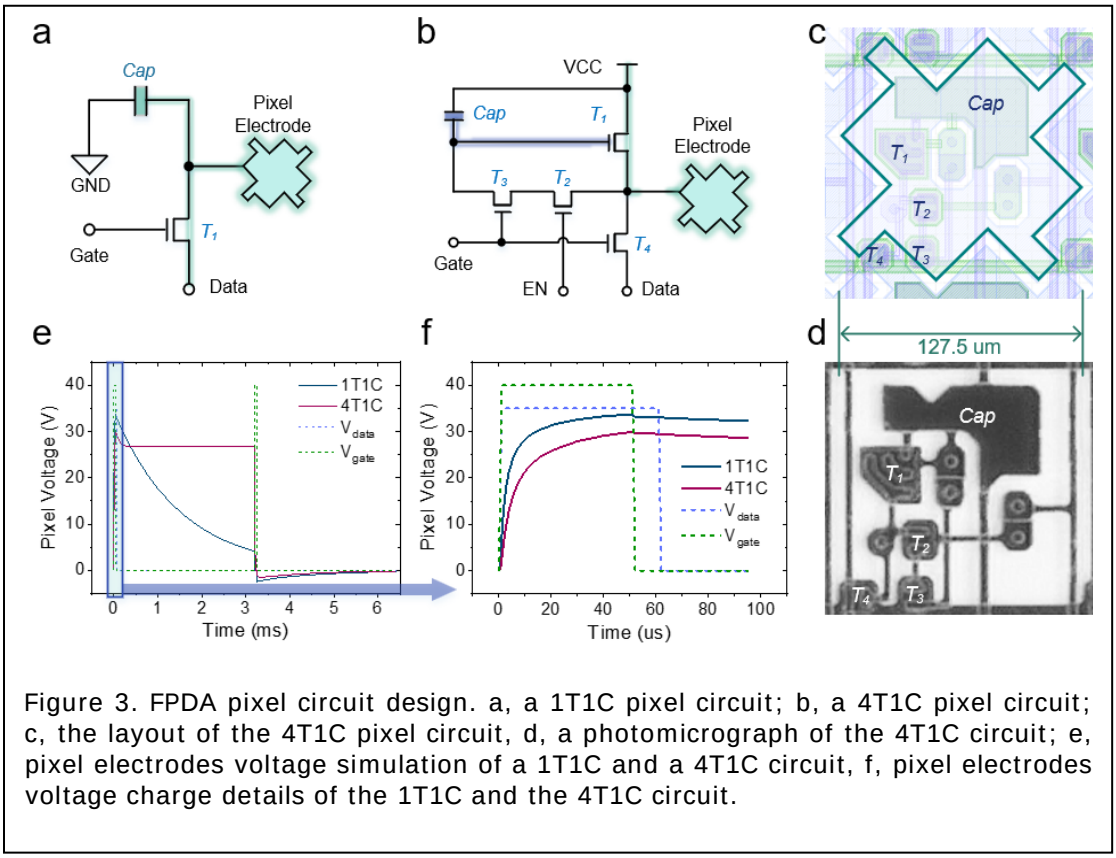

Figure 3. FPDA pixel circuit design. a, a 1T1C pixel circuit; b, a 4T1C pixel circuit; c, the layout of the 4T1C pixel circuit, d, a photomicrograph of the 4T1C circuit; e, pixel electrodes voltage simulation of a 1T1C and a 4T1C circuit, f, pixel electrodes voltage charge details of the 1T1C and the 4T1C circuit.

Pixel circuit design and simulation

Based on the improved TFT device design, the FPDA chips were optimised for pixel circuit operation. Presently, there are mainly two types of pixel circuits reported: the 1T1C[20] and the SRAM[25]. Generally, the 1T1C circuit is a simple passive circuit (shown in Fig.3a), while the SRAM is a complicated active circuit. In the 1T1C circuit, the pixel electrode is driven by the charge stored in the capacitor. As capacitor is a passive component, the stored charge will gradually leak out from the TFT and pixel electrode. When under the circumstances of high temperature or light exposure, the leakage current will rise by several orders of magnitude. In this case, the leakage rate of the stored charge will be accelerated, which will greatly reduce the pixel voltage and the driving force of droplets. To avoid this, a power signal needs to be introduced into the pixel circuit to realize active driving.

The SRAM is an ideal active circuit, the basic structure of which is bistable. The voltage of the pixel electrodes driven by the SRAM can remain constant, taking no account of the leakage current. Thus, the driving force on droplets can also be maintained continuously. So far there`s only one kind of SRAM circuit reported, which was designed by Sharp Life Science (EU) Ltd[25]. The downside of the reported SRAM circuit is that the circuit requires about 14 TFTs. Increasing the number of TFT devices in a pixel circuit results in the pixel layout sized of 210 μm. It is difficult to reduce the layout space of the SRAM circuit any further. The more TFT devices in the pixel circuit, the larger the layout space occupied by the pixel, and the more limitation of its applications, such as single-cell sorting and large-area FPDA chips.

Considering the factors of driving ability and layout space, we designed a pixel circuit with only 4 TFTs and a capacitor (named 4T1C) based on the commercialized amorphous silicon (a-Si) process. As shown in Fig.3b, a power source VCC has been introduced into the pixel circuit to maintain the driving voltage. The pixel size is 127.5 μm (shown in Fig.3c & 3d), which is much smaller than the reported SRAM circuit sized 210 μm[1] and the reported 1T1C circuit sized 1000 μm[20]. Fig.3e & 3f simulated

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the pixel voltage of 1T1C circuit and 4T1C circuit. As the 4T1C circuit introduces a VCC power to drive the pixel electrode; the charge stored in the capacitor only needs to keep the gate voltage stable. Compared with the 1T1C circuit, the 3T1C design reduces the leakage path of capacitor stored charge. Thus, the gate voltage of driver TFT (T1) tends to remain stable, enhancing the driving ability of the pixel voltage.

When we fabricate the FPDA chip, except the design of TFT device and array circuits, there are also some items to be carefully considerate. Table 1 summarized the recommended specifications of different items of the FPDA chip, including the fabrication process parameters of the backplane glass substrate and the cover ITO glass. These parameters are obtained by continuous optimization and iteration of FPDA chip design, and have been verified the effectiveness by experiments. In this work, we have followed the recommended specifications to ensure the performance of FPDA chip.

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Table 1, Summary of the recommended specifications to fabricate the FPDA.

Components	Structure	Items	Recommended Specifications	This work
Substrate	TFT	Ion	≥1E-6A	1E-5A
		Ioff	≤1E-10A	5E-11A
		Vth	0±5V	0~4V
		SS	≤2V/dec	1~2V/dec
		μ	≥0.5cm²/(V·S)	0.55cm²/(V·S)
	Metal	Sheet resistance	≤0.5Ω/□	0.4Ω/□
	Dielectric	εr	≥5.5	6~7
		Breakdown strength	≥2MV/cm	2~3MV/cm
	Surface	Equal height area ratio	≥60%	60%
		Surface height difference	≤5% gap	5%
	Outline	X/Y tolerance	±0.15mm	±0.12mm
		Z tolerance	±0.05mm	±0.04mm
	Hydrophobic Layer	Contact angle	≥110°	120°
Cover plate		Rolling angle	≤20°	15°
	ITO	Surface height difference	≤50nm	30~40nm
		Sheet resistance	≤100Ω/□	80Ω/□
		Transmittance	≥85%	90%
	Inlet/outlet hole	Diam tolerance	±5%diam	±3%
		Location tolerance	±50um	±50um
	Outline	X/Y tolerance	±0.15mm	±0.15mm
		Z tolerance	±0.05mm	±0.04mm

Field Programmable Droplets Array for concentration gradients generation

Traditional IFC microfluidics are generally based on physical micro-channels. Comparatively, FPDA chips have no prefabricated micro-channels, thus the liquid manipulation process is quite different. On the traditional IFC microfluidics platform, the droplets are generated by the coordination of pumps and micro-channels. The flow path and volume of droplets on IFC microfluidics is commonly fixed and restricted, and it`s difficult to address and manipulate the target droplet. However, with FPDA chips, each individual droplet is addressable, and its volume can be controlled. The array scale of FPDA chips is much larger than that of the traditional IFC microfluidics. The massive pixels in the AM array pave the way for high-throughput and versatile

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reaction of liquid droplets, providing the ability to split, sort, and merge different sizes of droplets freely and dynamically. These liquid operations are routine on the FPDA chips, whilst being almost impossible using traditional microfluidic chips.

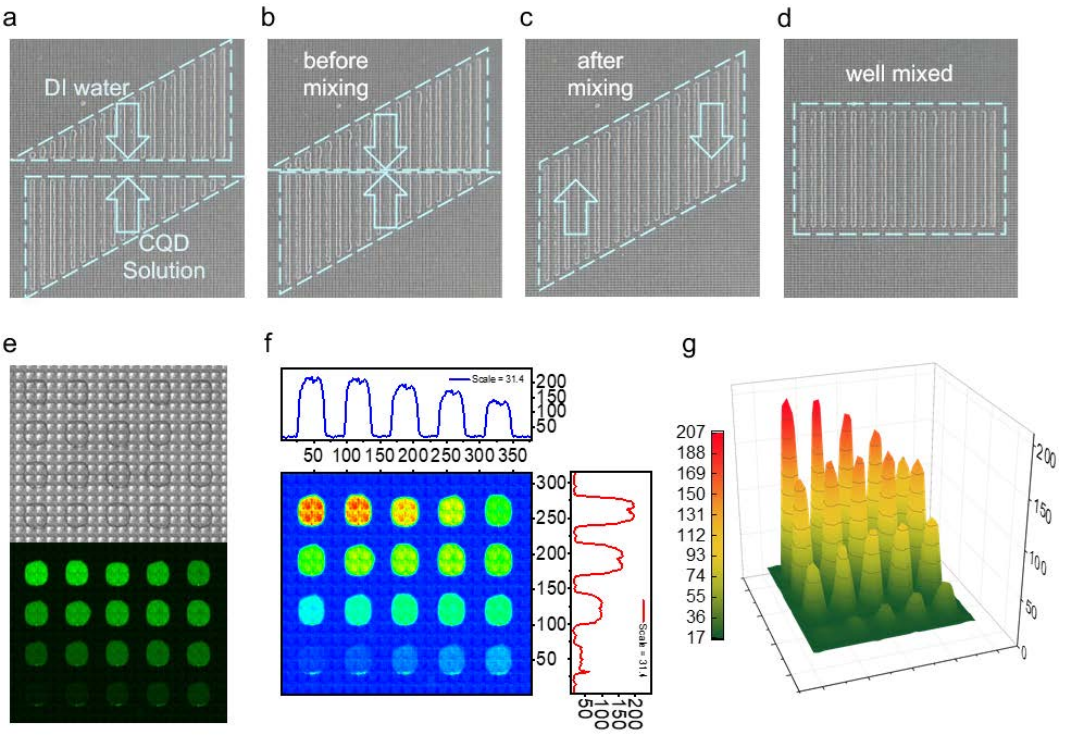

Figure 4. Virtual channel microfluidics and droplets fluorescence intensity gradient. a, virtual channel of DI water and CQDs fluorescent solution in different length; b ~ d, Mixing of DI water and CQDs fluorescent solution; e, Bright field and fluorescence images of fluorescent solution with different concentration gradients; f, intensity value extracted from the fluorescence image; g, Stereoscopic image of fluorescent solution with different concentration gradients.

To further showcase the application scenarios of FPDA chips, an experiment was designed to realize different concentration gradients of Carbon quantum dots (CQDs) fluorescent solution. As shown in Fig.4a, liquid droplets were generated in various pixel size, which looks like they are being arranged by virtual channels. the droplets were then mixed by moving them back and forth to mix the reagent evenly (shown in Fig.4b~4d). Fig.4e&4f show the bright field and fluorescence image of fluorescent solution with different concentration gradients. The fluorescence intensity value of different droplets has also been extracted in Fig.4g, 4h. It can be seen that, the 20 droplets have relatively different concentrations to each other, indicating that the AM-

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FPDA chip could realize a high-throughput concentration gradient by the virtual channel.

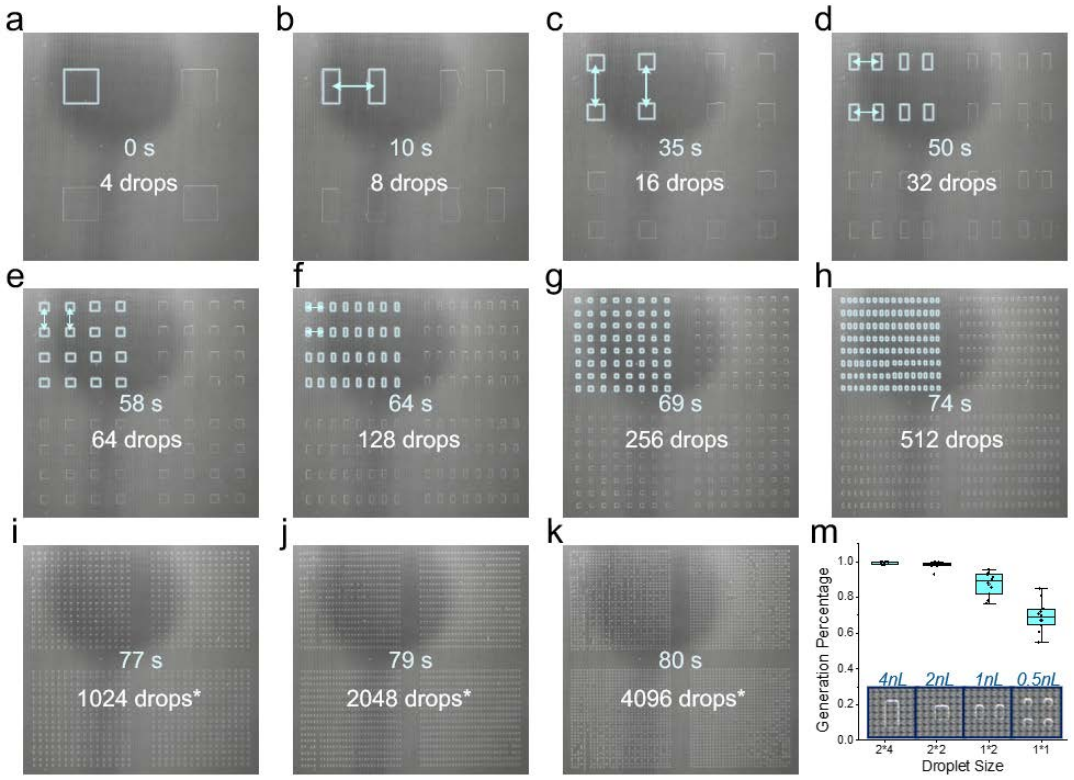

Figure 5. High-throughput droplets array generation process and generation percentage. a~k, the generation step time of different droplets size. m, generation success percentage of different droplets size.

Concentration gradients generation

To realize the best control precision and highest array usage efficiency of FPDA chip, it`s necessary that a single pixel can drive a single droplet independently. The one-to-two droplets generation method has been applied to generate massive individual droplets in a short time. The bisection generation principle is simple and effective, one droplet subdivides into two, then two droplets divide into four, and so on. In this way, the number of single droplets can be increased exponentially (Supplementary Section 5). Fig.5a~5k shows the droplets generation process using the bisection method, and the time interval of each step is about 0.5s. Based on the bisection generation method, one droplet can be divided into two continuously. Under the control of AM electrode array, thousands of single droplets can be obtained in about 80s. As the

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pixel number of the FPDA chip is 65,536, it`s capable of generating more than four thousand droplets array (shown in Fig.5k).

The droplet manipulation principle of FPDA chips is based on EWOD, which is sensitive to the driving signals and interface state. In the bisection process, the droplet volume keeps halving, while the pixel pitch is invariable. Therefore, the droplet would gradually approach the limit size that cannot be bisected. Fig.5m illustrates the generation percentage of droplets in different sizes. The size was defined by the number of pixels occupied by the droplet. When the droplet size is larger than 2x2, the success rate of droplets generation was close to 100%. When the droplet sized 2x2 divided into two droplets sized 1x2, the success rate would reduce to about 90%. The single pixel droplet was the most difficult to be generated, whose typical success rate was about 70%. As there is a limit in the minimum size of droplets that can be generated by FPDA, which is related to the ratio of gap to droplet size. When the single-pixel droplet is generated, the droplet size is close to the limit to split, the force of EWOD is unable to break through the critical value of the surface tension, leading to the failure of single droplet generation.

Conclusions

In conclusion, we have demonstrated a robust and powerful tool for generating and manipulating micro-droplets, namely the FPDA platform. The FPDA chip possesses 65,536 pixels and could realize high throughput droplets generation and manipulation at the single pixel level. All the droplets can be addressed and manipulated independently, with the minimum droplet volume of about 0.5 nL. The potential of the FPDA platform is to revolutionize applications in point-of-care diagnostics, drug development, and environmental monitoring. The high accuracy and real-time capabilities of FPDA chips offer greater sensitivity and specificity for detection and analysis of biomolecules and cells. Integration of multiple functionalities on a single chip could lead to new miniaturized analytical tools that are more accurate, efficient, and sensitive than current technologies. This work shows the great application

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potential of TFT technology in FPDA platform, to create new breakthroughs for the lab-on-a-chip systems. Based on the FPDA chip, the droplet analysis system could be further miniaturized along with a higher throughput. Our study serves as a foundation for future research aiming to optimize droplet manipulation techniques and unlock the full potential of FPDA-based microfluidic devices for future breakthroughs.

Methods

The Carbon Quantum Dots solutions were purchased from Suzhou Xingshuo Nanotech Co., Ltd. (Suzhou, P.R.China), the concentration of 10 mg/mL, the extraction wavelength of 480 nm, the photoluminescent wavelength of 514 nm.

FPDA device fabrication.

We designed and fabricated the FPDA device. The fabrication process of TFT-based FPDA is similar with the backplane of flat panel display, both of which are fabricated by thin film electronic technology and photolithography process. The structure of FPDA device is shown in Fig. 1a & 1b, the amorphous silicon TFT array was fabricated on a glass substrate, an electrowetting dielectric layer (300 nm SiNx) and a hydrophobic layer was deposited on the top of the TFT array. A plastic spacer (not shown in Fig. 1b) was used to define the gap (30 μm) between the bottom glass substrate and the ITO coated cover glass plate. The side of the ITO layer facing the bottom was also coated with a thin layer of hydrophobic material. The conductive ITO was constantly connected to the system ground, and a direct electric field was formed across the gap when a corresponding pixel located at the bottom is selected. The surrounding medium oil was used to suppress liquid droplet evaporation and enhance droplet mobility.

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Electronics system.

The FPDA device features an active-matrix array of 256 × 256 elements, totalling to 65536 addressable pixel electrodes. We use a MUX to separate 1 column signal into 4 columns. The MUX contains 4 TFTs controlling each TFT to open in sequence. The row signals is generated by the described GOA circuits. The GOA circuits require 4 driver signals, namely CK, CKB, STV and RST. The CK and CKB is two inversion clock signals; The STV is a stimulus signal to stimulate the GOA circuits; The RST is a reset signal to reset all the output signals of the GOA circuits. The FPDA needs 64 column signals and 4 GOA signals. We use a DC-DC power to supply the voltage for the FPDA platform, and a STM32 embedded system to control the driving signals.

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Author Contributions

D.W., K.J. and H.M. conceived the concept and experiments. D.W., K.J., C.H. M.D. and S.S. carried out the experiments, D.W., Y.B., J.L., S.H. and J.Y. collected and analysed the data. D.W., K.J. A.N. and H.M. wrote the manuscript, and all authors reviewed and commented on the manuscript.

Competing interests

Patents based on this research have been submitted.

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